Remarks:

Reconsideration of the application is requested.

Claims 1-4 and 6-12 remain in the application. Claim 1 has been amended. A marked-up version of claim 1 is attached hereto on a separate page. Claim 5 has been cancelled. Claims 10-12 have been withdrawn.

In the last paragraph on page 2 of the Office action, claims 1, 2, 4, and 8 have been rejected as being fully anticipated by Ryan et al. (U.S Patent No. 5,972,788) under 35 U.S.C. § 102.

Claim 1 has been amended to include the subject matter of claim 5, therefore the rejection over Ryan et al. under 35 U.S.C. § 102 is now moot.

In the third paragraph on page 4 of the Office action, claims 3, 5-7, and 9 have been rejected as being obvious over Ryan et al. (U.S Patent No. 5,972,788) in view of Leung et al. (U.S Patent No. 5,563,762) under 35 U.S.C. § 103.

The rejections have been noted and the claims have been amended in an effort to even more clearly define the invention of the instant application. The claims are patentable for the

reasons set forth below. Support for the changes is found in claim 5 of the instant application.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 1 calls for, *inter alia*:

the second metal layer having an electrically conductive connection between the third metal area and the fourth metal area.

The Ryan et al. reference discloses an electronic device including an interconnect and a capacitor, both including respective portions of a first metal layer, a dielectric layer and a second metal layer, and further including a connection to both the first metal layer and the second metal layer of the interconnect and a connection to each of the first metal layer and the second metal layer of the capacitor (column 3, lines 55-62).

The object of Ryan et al. is to form a metal-to-metal **precision capacitor** and interconnects resistant to metal migration in the same process (column 3, lines 39-42). A precision capacitor is a capacitor for analog circuits. Furthermore, Ryan et al. state that "While such a variation in

capacitance and voltage limitation is generally tolerable in digital circuits, there are many types of analog circuits in which variation in capacitance with voltage is not tolerable and requires metal plates to increase carrier concentrations" (column 3, lines 12-17).

Therefore, a person of ordinary skill in the art would consider the capacitor of Ryan et al. as a capacitor for analog devices. This point of view is further supported by the statement that "such a capacitor plate is generally **at least several times** the width of a conductor" (column 6, lines 7-10).

Contrary thereto, a capacitor forming a memory element is typically very small, since memory elements are tightly packed to obtain a high memory density.

Furthermore, the word "memory" is only used in conjunction with information storage, as the enclosed pages of The Random House Dictionary and Semiconductor Memories indicate.

Therefore, contrary to the Examiner's opinion, applicants do not consider the capacitor of Ryan et al. to be a memory element.

The combination of Ryan et al. and Leung et al. would not lead to the invention of the instant application as recited in claim 1 of the instant application for the following reasons.

Ryan et al. disclose the formation of interconnects comprising two metal layers, which are insulated from each other by a dielectric layer. This dielectric layer is the key in overcoming the problems associated with electromigration and metal migration (column 6, lines 39-46). Therefore, a person of ordinary skill in the art would be taught to integrate a dielectric layer between two metal layers.

Contrary thereto, Leung et al. allow a direct connection between the metal areas (126) and the metal layer (134), which contradicts the teaching of Ryan et al..

Furthermore, a person of skill in the art would have had to remove the mandatory dielectric layer of Ryan et al. in order to allow an electrical connection of the upper metal layer (134) from underneath.

Finally, Leung et al. teach placing the capacitor on top of the passivation layer of an otherwise completed integrated circuit (column 3, lines 45-48). Therefore, an interconnect simultaneously formed with a capacitor as disclosed in Ryan et al. is explicitly excluded by the teaching of Leung et al..

Regarding the second metal layer having an electrically conductive connection between the third metal area and the fourth metal area, as recited in claim 1, it is noted that Ryan et al. simultaneously form an interconnect and a capacitor. There is no electrical connection by either of the two metal layers M1 and M2 and either of the electrodes of the capacitor and the interconnect. Furthermore, Ryan et al. provide no motivation for such a direct connection.

Another aspect refers to the kind of electrical connection of the upper and lower electrode. The upper and lower electrodes (21 and 22) are directly contacted by metal studs (14 and 32), respectively. According to the arguments provided by the Examiner, a person of ordinary skill in the art would leave an electrical connection between the upper electrode (22) and the upper layer (25) of the interconnect (23) to provide a contact area to contact the upper electrode (22) in view of Leung et al. Applicants disagree with this assertion for the following reasons.

Leung et al. provide an on-chip capacitor. Therefore, a simultaneous formation of an interconnect contradicts the teaching of Leung et al.. A person of ordinary skill in the art would not combine the teachings of Ryan et al. with those of Leung et al..

On the other hand, if a person of ordinary skill in the art would place the capacitor on top of a chip, no insulating layer covering the contact area and the memory element and having at least one opening formed therein and leading to said contact area, as recited in claim 1 of the instant application would be present.

Finally Ryan et al. already disclose how to connect the upper electrode. This is accomplished by a direct connection with a metal stud formed within an inter-level dielectric (31). However, Ryan et al. do not present any motivation, which would lead a person of ordinary skill in the art to provide a metal area outside the upper electrode, which can be used to contact the upper electrode. An electrical connection between the upper electrode (22) and the upper metal layer (25) of the interconnect (23), which might be used as such a contact area is far beyond the scope of Ryan et al.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1. Claim 1 is, therefore, believed to be patentable over the art and since all of the dependent claims are ultimately dependent on claim 1, they are believed to be patentable as well.

In view of the foregoing, reconsideration and allowance of claims 1-4 and 6-9 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel respectfully requests a telephone call so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made.

Please charge any fees which might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner & Greenberg P.A., No. 12-1099.

Respectfully submitted,

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For Applicant(s)

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Marked-up version of the claims:

Claim 1 (amended). A semiconductor component, comprising:

a first metal layer forming a first metal area and a second metal area electrically insulated from one another;

a dielectric layer;

a second metal layer produced separately from said first metal layer and forming a third metal area insulated from said first metal layer by an interposition of said dielectric layer, and said third metal area together with said dielectric layer and said first metal area forms a memory element, said second metal layer further forming a fourth metal area which together with said second metal area forms a contact area used to make contact with said second metal layer and said second metal layer having an electrically conductive connection between said third metal area and said fourth metal area;

an insulation layer covering said contact area and said memory element and having at least one opening formed therein and leading to said contact area; and

an electrically conductive material filling said opening for making contact with said second metal layer.